CLAIMS

1. A method of calculating a Cyclic Redundancy Check (CRC) value for a multi-bit input data word, using a defined generator polynomial having a length, the method comprising:

a) serially shifting at least a portion of the input data word into a register;

b) XORing contents of the register with the generator polynomial if an LSB of the register is '1';

c) shifting the contents of the register right by one position;

d) shifting into an MSB position of the register a new bit of the input data word, having been XORed with the LSB of the register;

e) repeating step d) for all message data bits of the input data word;

f) shifting into the register a number of '0's equal to the length of the generator polynomial; and

g) reading from the register the calculated CRC value.

2. The method of claim 1, further comprising generating a pseudo-random noise (PN) sequence using the calculated CRC value.

3. The method of claim 1, further comprising Turbo coding input data using the calculated CRC value.

4. The method of claim 1, further comprising convolutionally coding input data using the calculated CRC value.

5. An apparatus for calculating a Cyclic Redundancy Check (CRC) value for a multi-bit input data word, using a defined generator polynomial having a length, comprising:

a register for serially receiving at least a portion of the input data word;

an XOR gate for XORing contents of the register with the generator polynomial if an LSB of the register is '1';

means for shifting the contents of the register right by one position;

means for repeatedly shifting into an MSB position of the register a new bit of the input data word, having been XORed with the LSB of the register, until all bits of the input data word have been shifted into the register; and

means for shifting into the register a number of '0's equal to the length of the generator polynomial.

6. A microprocessor unit for calculating a Cyclic Redundancy Check (CRC) value for a multi-bit input data word, using a defined generator polynomial having a length, comprising:

a register for serially receiving at least a portion of the input data word;

an XOR gate for XORing contents of the register with the generator polynomial if an LSB of the register is '1';

first means for shifting the contents of the register right by one position;

second means for repeatedly shifting into an MSB position of the register a new bit of the input data word, having been XORed with the LSB of the register, until all bits of the input data word have been shifted into the register; and

third means for shifting into the register a number of '0's equal to the length of the generator polynomial.

7. A microprocessor unit according to claim 6 wherein the register, XOR gate, and first, second, and third means are part of an apparatus for calculating the CRC value that is arranged to be operated in response to a single instruction.

8. A method of calculating a check value for a multi-bit input data word, using a defined generator polynomial having a length, the method comprising:

serially shifting at least a portion of the input data word into a register;

XORing contents of the register with the generator polynomial if a bit in a first bit position of the register is a first value;

shifting the contents of the register by one position;

serially shifting into a second bit position of the register a new bit of the input data word, the new bit having been XORed with a bit in the first bit position of the register;

shifting into the register a number of second values; and

reading from the register the calculated check value.

9. The method of claim 8, further comprising generating a pseudo-random noise (PN) sequence using the calculated check value.

10. The method of claim 8, further comprising Turbo coding input data using the calculated check value.

11. The method of claim 8, further comprising convolutionally coding input data using the calculated check value.